IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A ferro-electric random access memory comprising:

a memory cell having a first ferro-electric capacitor;

a sense amplifier which determines a data value of the memory cell by using a reference electric potential; and

a reference electric potential generating circuit which generates the reference electric potential by using a paraelectric capacitor and a second ferro-electric capacitor;

wherein one end of the paraelectric capacitor and one end of the second ferro-electric capacitor are connected to a common node, a first driving signal is supplied to the other end of the paraelectric capacitor, and a second driving signal is supplied to the other end of the second ferro-electric capacitor.

Claim 2 (Canceled).

Claim 3 (Currently Amendedl): The ferro-electric random access memory according to ~~claim 2~~ claim 1, further comprising:

bit lines; and

selective transistors connected between the bit lines and the common node.

Claim 4 (Currently Amended): The ferro-electric random access memory according to ~~claim 2~~ claim 1, further comprising:

a trimming circuit to finely adjust values of the first and second driving signals.

Claim 5 (Original): The ferro-electric random access memory according to claim 1, wherein the reference electric potential generating circuit is disposed in the memory cell array.

Claim 6 (Original): The ferro-electric random access memory according to claim 1, wherein the reference electric potential generating circuit is disposed at the peripheral portion of the memory cell array.

Claim 7 (Currently Amended): The ferro-electric random access memory according to ~~claim 2~~ claim 1, further comprising:

a voltage follower circuit which generates a first electric potential ~~having current driving force~~ on the basis of an electric potential of the common node.

Claim 8 (Original): The ferro-electric random access memory according to claim 7, further comprising:

a trimming circuit which generates a second electric potential that finely adjusts a value of the reference electric potential; and

an adder which adds the first and second electric potentials.

Claim 9 (Currently Amended): A ferro-electric random access memory comprising:

a memory cell having a first ferro-electric capacitor;

a sense amplifier which determines a data value of the memory cell by using a reference electric potential;

a reference electric potential generating circuit which generates the reference electric potential by using a second ferro-electric capacitor; and

a trimming circuit which outputs an output electric potential that finely adjusts the value of the reference electric potential;

wherein one end of the second ferro-electric capacitor is connected to a common node, and a driving signal is supplied to the other end of the second ferro-electric capacitor.

Claim 10 (Canceled).

Claim 11 (Currently Amended): The ferro-electric random access memory according to ~~claim 10~~ claim 9, further comprising:

bit lines; and

selective transistors connected between the bit lines and the common node.

Claim 12 (Currently Amended): The ferro-electric random access memory according to claim 9, wherein the trimming circuit ~~includes a component by a paraelectric capacitor, and~~ finely adjusts the value of the reference electric potential ~~in consideration of the component~~ based on a signal that is generated by a paraelectric capacitor.

Claim 13 (Original): The ferro-electric random access memory according to claim 9, wherein the reference electric potential generating circuit is disposed in the memory cell array.

Claim 14 (Original): The ferro-electric random access memory according to claim 9, wherein the reference electric potential generating circuit is disposed at the peripheral portion of the memory cell array.

Claim 15 (Currently Amended): The ferro-electric random access memory according to ~~claim 10~~ claim 9, further comprising:

a voltage follower circuit which outputs an output electric potential ~~having current driving force~~ on the basis of an electric potential of the common node.

Claim 16 (Original): The ferro-electric random access memory according to claim 15, further comprising:

an adder which adds the output electric potential of the trimming circuit and the output electric potential of the voltage follower circuit.

Claim 17 (Currently Amended): A read method of a ferro-electric random access memory, comprising:

pre-charging first and second bit lines when data is read from a memory cell having a first ferro-electric capacitor;

changing an electric potential of the first bit line in accordance with a value of the data;

generating a reference electric potential by using a paraelectric capacitor and a second electric capacitor;

setting an electric potential of the second bit line to the reference electric potential; and

determining the value of the data on the basis of a potential difference between the first and the second bit lines;

wherein the reference electric potential is generated due to a first driving signal being supplied to the other end of the paraelectric capacitor, and a second driving signal being supplied to the other end of the second ferro-electric capacitor;

wherein values of the first and second driving signals are finely adjusted by a trimming circuit.

Claims 18 - 19 (Canceled).

Claim 20 (Currently Amended): The read method according to claim 17, wherein the reference electric potential ~~becomes an electric potential having current driving force by~~ is supplied to a voltage follower circuit.

Claim 21 (Original): The read method according to claim 20, wherein the value of the reference electric potential is finely adjusted by a trimming circuit.